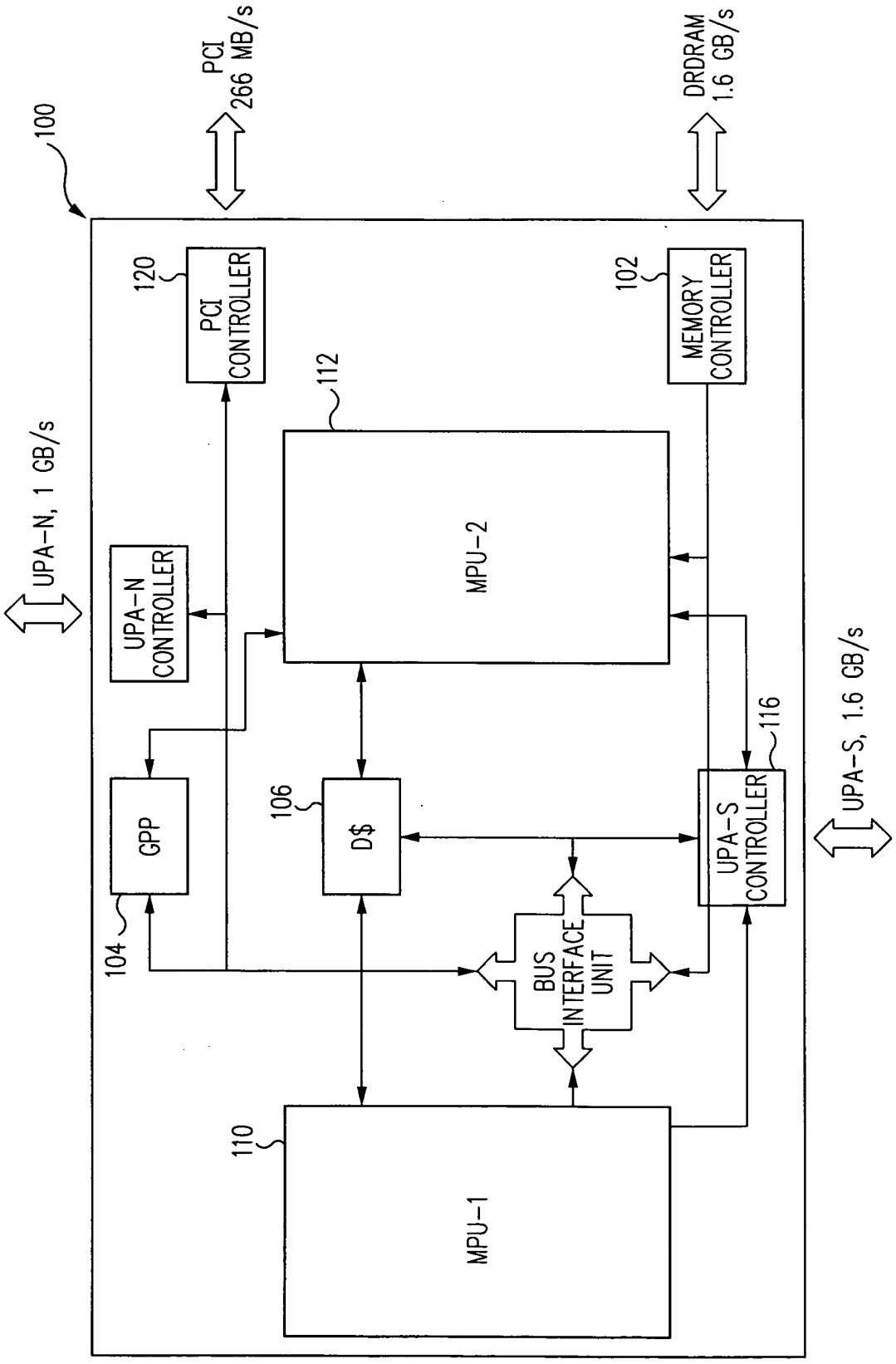
100
PCI
266 MB/s
DRDRAM
1.6 GB/s
120
PCI CONTROLLER
102
MEMORY CONTROLLER
112
MPU-2
UPA-N, 1 GB/s
UPA-N CONTROLLER
GPP
104
106
D$
116
UPA-S CONTROLLER
UPA-S, 1.6 GB/s
BUS INTERFACE UNIT
110
MPU-1

FIG. 1A

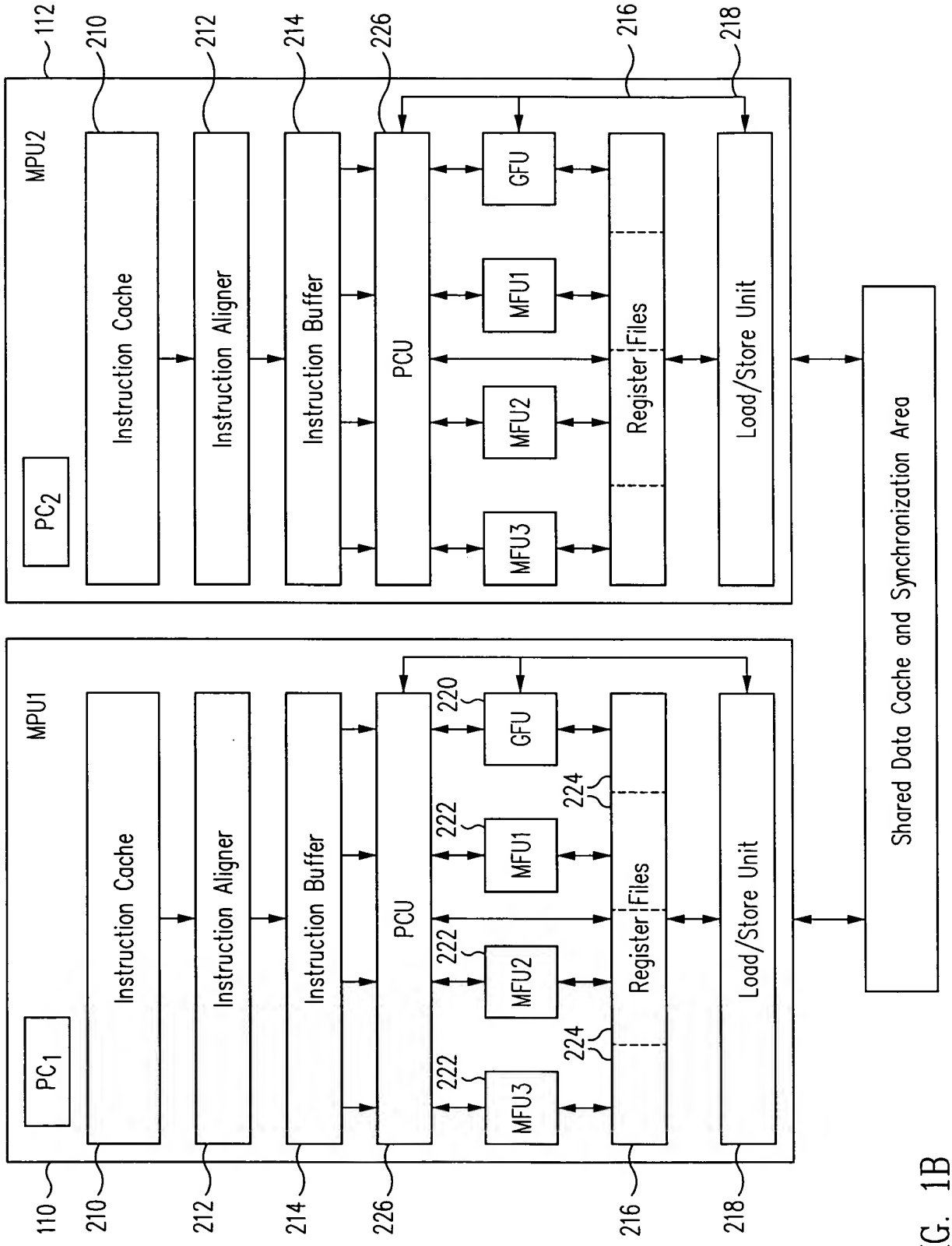
MPU2
112
210
212
214
226
216
218
PC2
Instruction Cache
Instruction Aligner
Instruction Buffer
PCU
GFU
MFU1
MFU2
MFU3
Register Files
Load/Store Unit
MPU1
PC1
220
222
224
Shared Data Cache and Synchronization Area
110

FIG. 1B

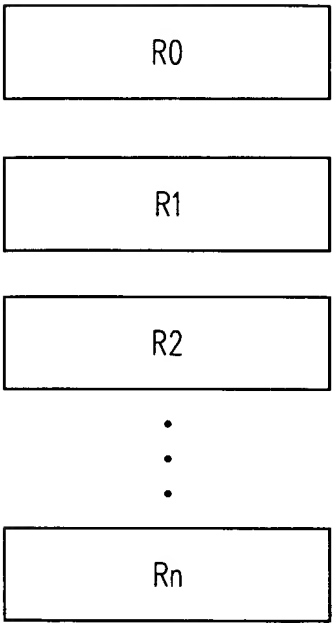

FIG. 2A

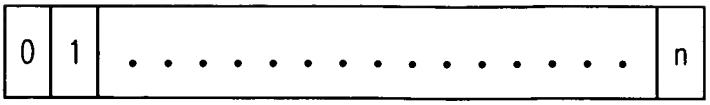

FIG. 2B

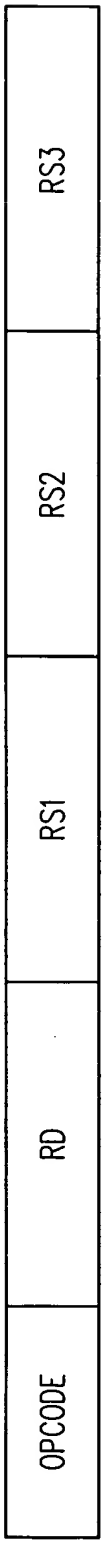
OPCODE
RD
RS1
RS2
RS3

FIG. 3A

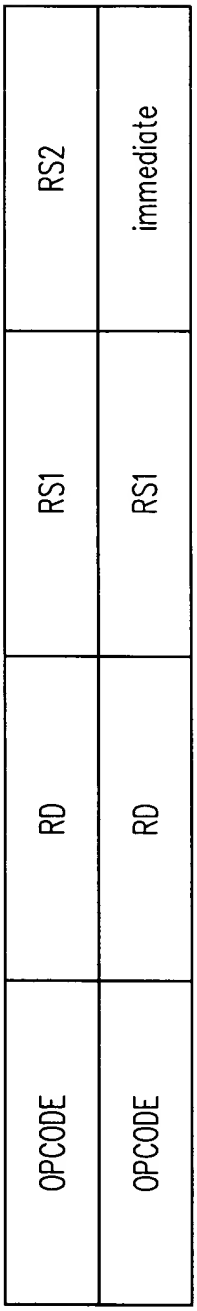
OPCODE
RD
RS1
RS2
OPCODE
RD
RS1
immediate

FIG. 3B

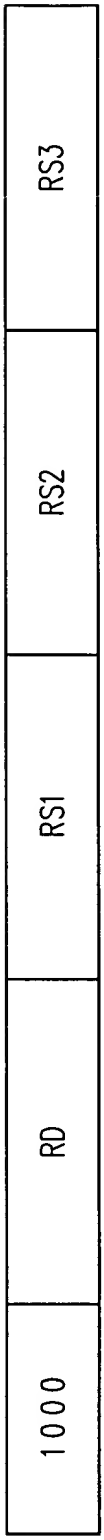

FIG. 4A

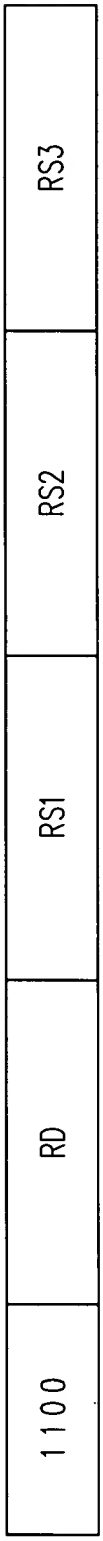

FIG. 4B

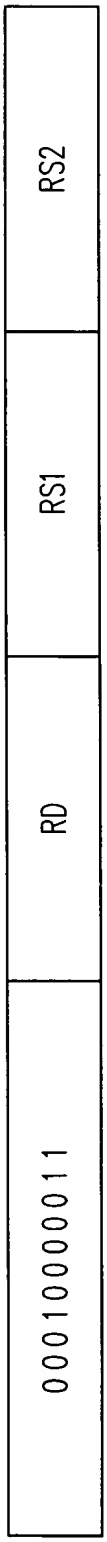

FIG. 4C

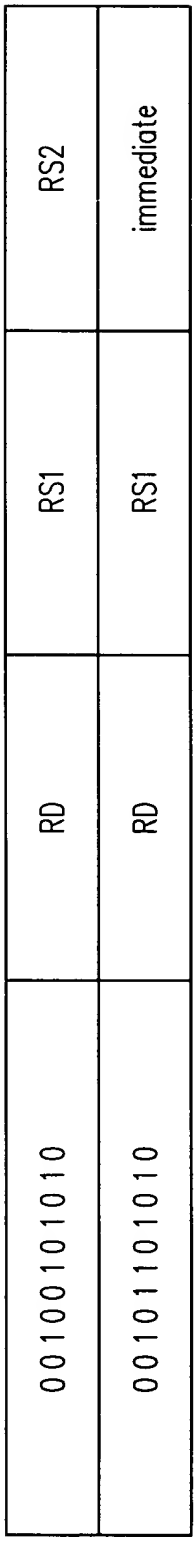

FIG. 4D

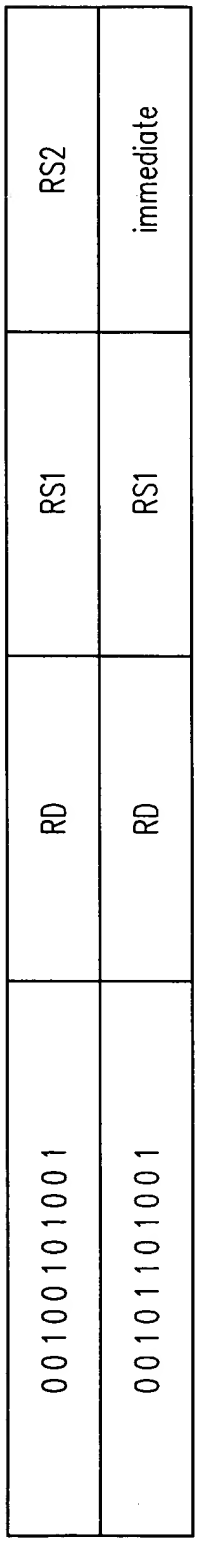

FIG. 4E

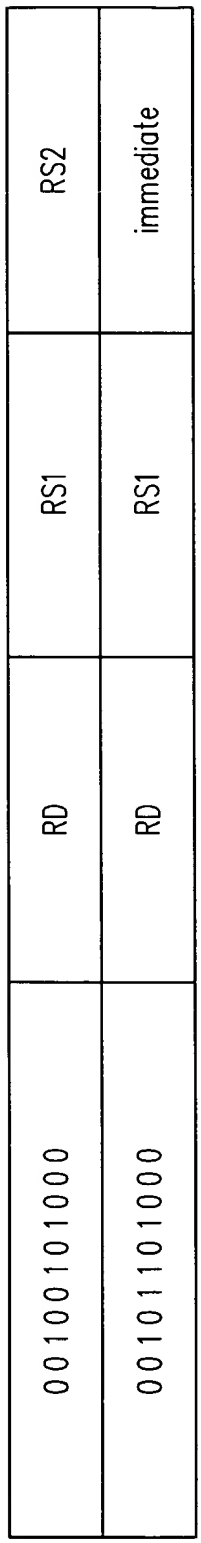

FIG. 4F

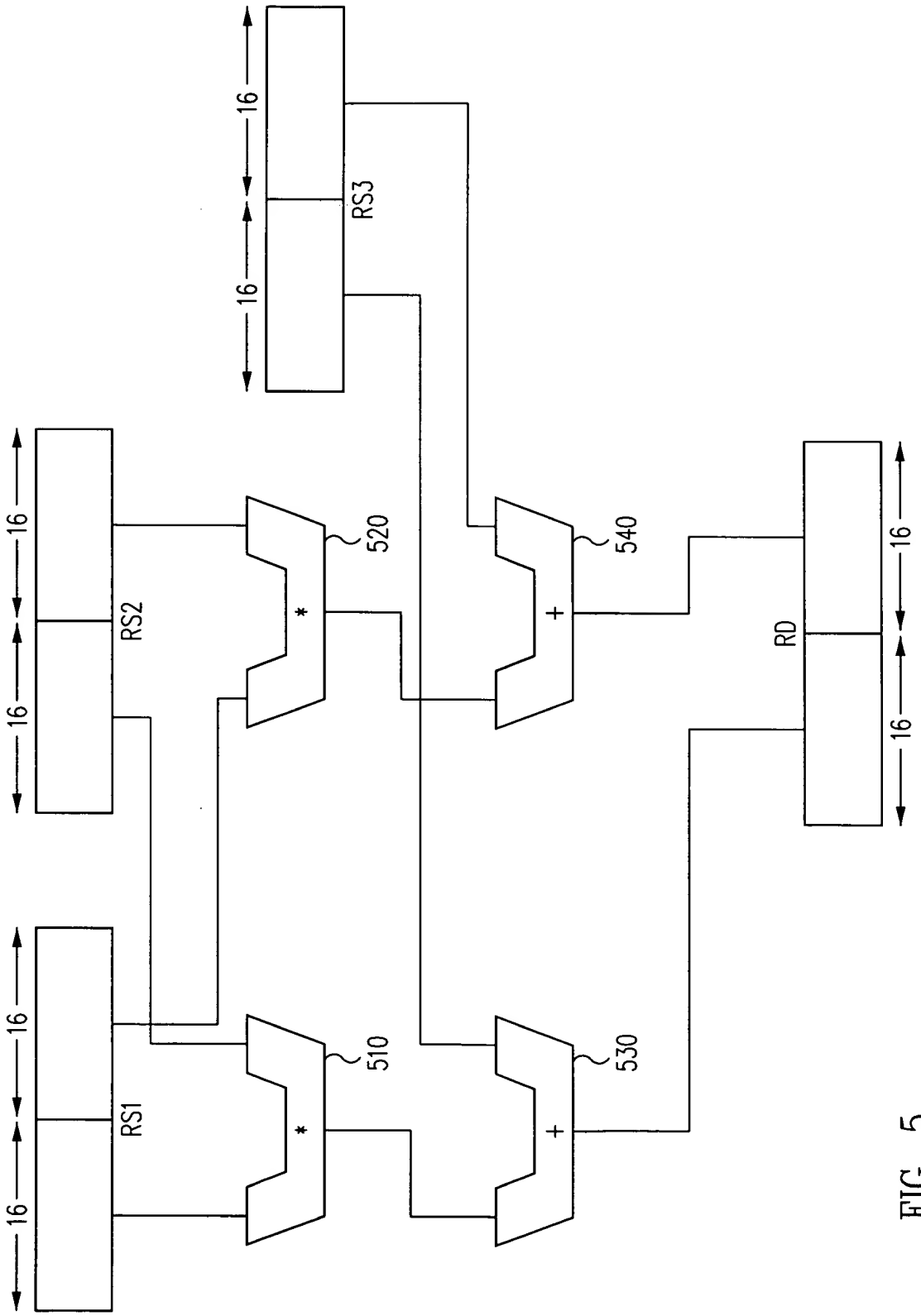

FIG. 5

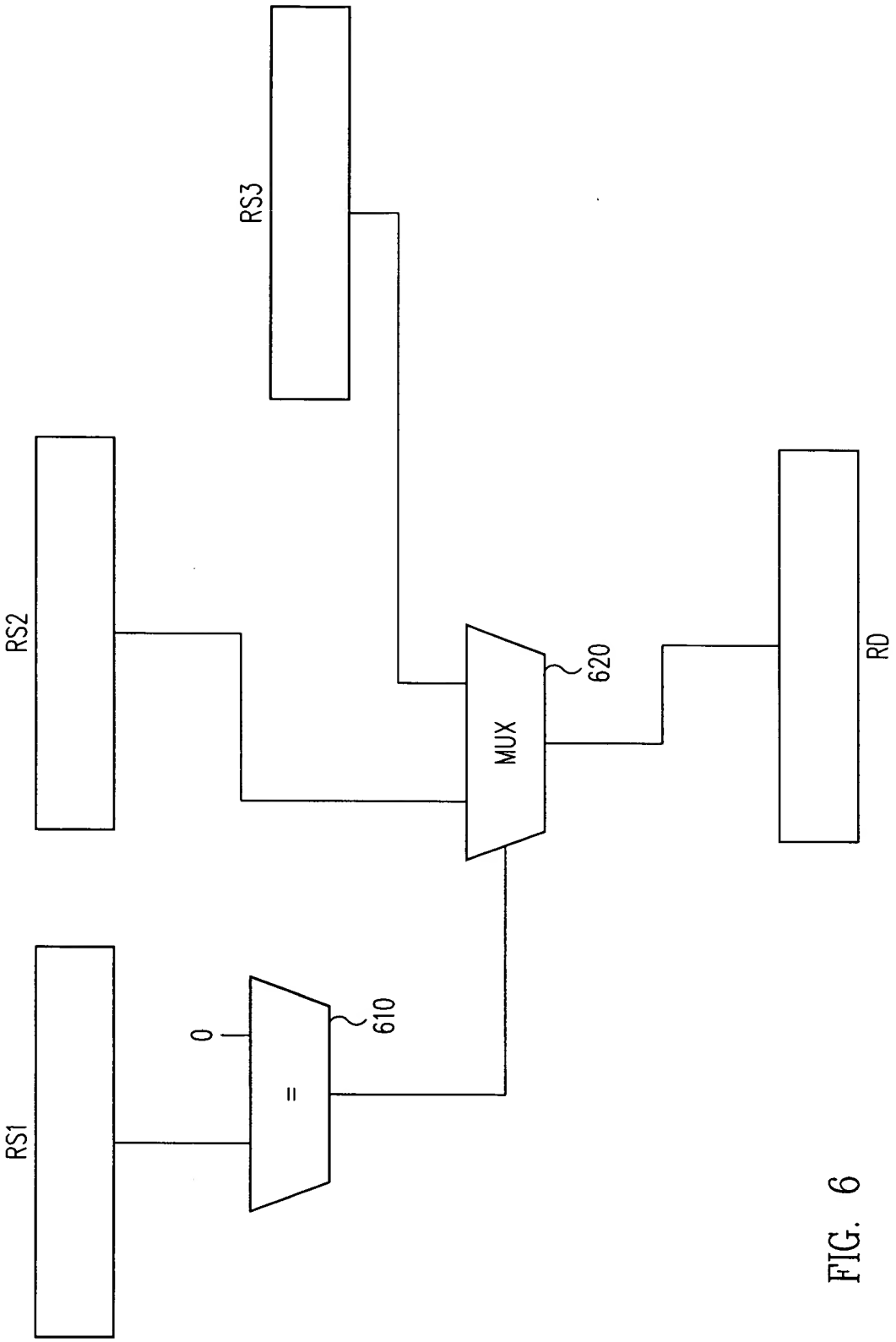

FIG. 6

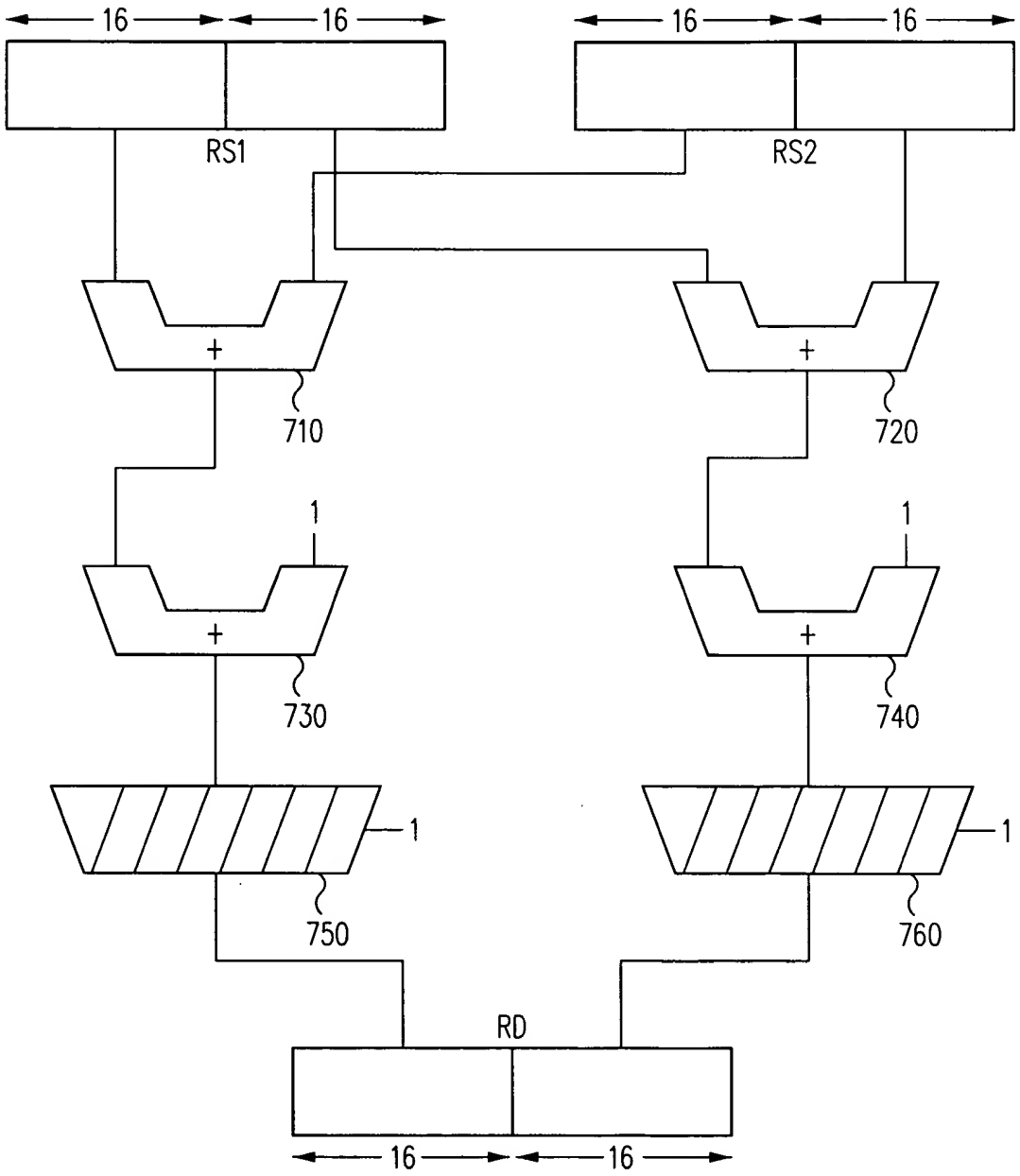

FIG. 7

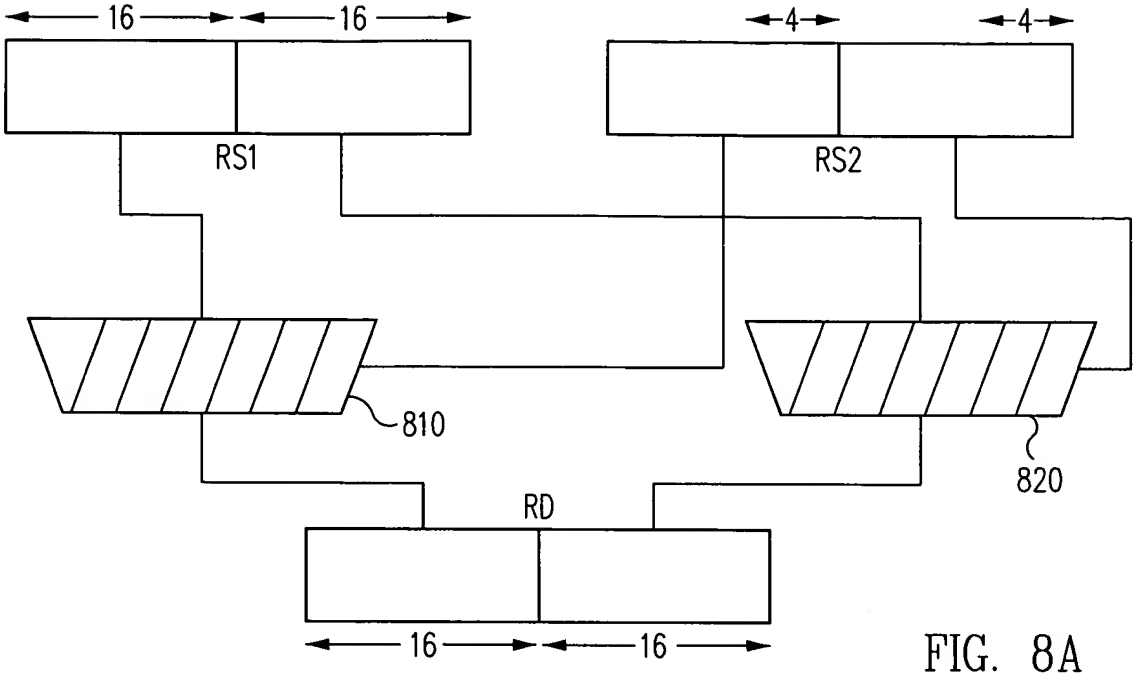
16
16
4
4
RS1
RS2
810
820
RD
16
16

FIG. 8A

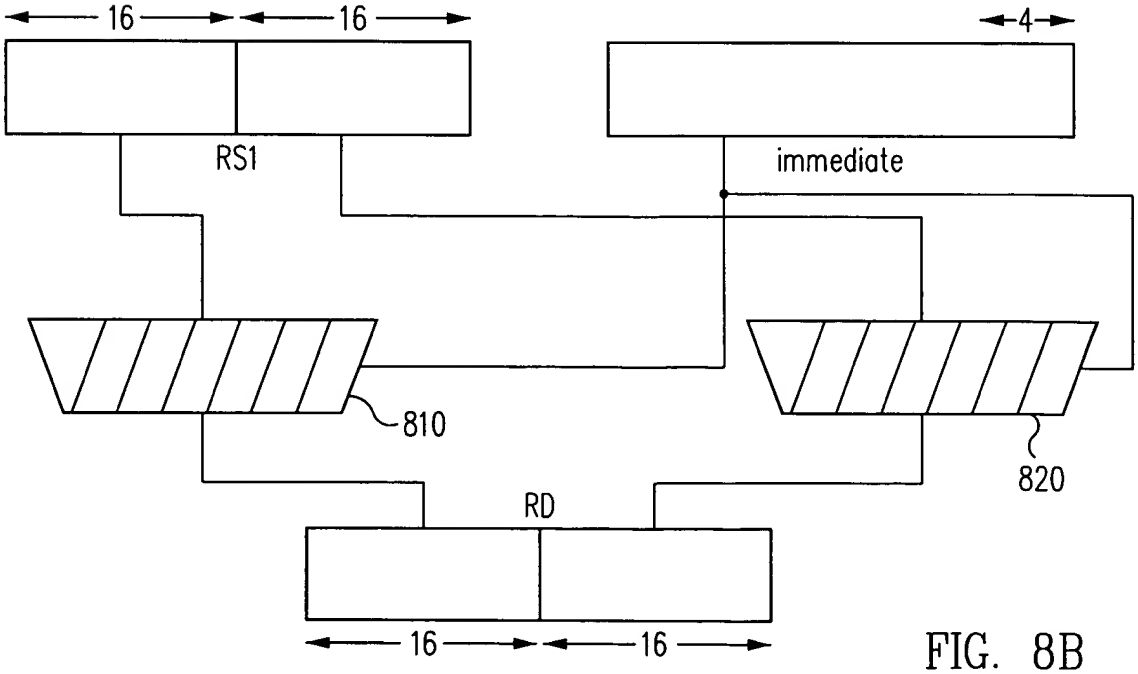
16
16
4
RS1
immediate
810
820
RD
16
16

FIG. 8B